REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-29 are pending. Claims 1-29 stand rejected.

No claims have been amended. No claims have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-5, 14-18, 21-24, 27 and 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over "Value Speculation Scheduling for High Performance Processors" by Fu et al. ("Fu").

Fu discloses completely different value prediction techniques than the one claimed by Applicants. Fu discloses a value predictor that predicts a value of a specific instruction using merely history data of this specific instruction, without using any information determined in the dependency chain prior to the specific instruction (Fu, p. 265, lines 6- 27).

In the presently claimed invention, in contrast, a data ("outcome") determined earlier in the dependency chain ("second instruction"), is used as input (" a key ") into a software structure, to actually predict the outcome of a first instruction.

Further, the Examiner acknowledges that Fu " does not expressly disclose the limitation wherein the outcome of the second instruction represents a key into a software structure that includes a set of keys and a corresponding set of predicted outcomes of the first instruction". However, the Examiner cites a table of predicted values in Fu for such teaching, contending that " it would have been apparent for one of ordinary skill in the art at the time the invention was made that the index or key into the table disclosed by Fu could be designated as the outcome of the second instruction, or any such value, so long as unnecessary conflicts are avoided".

Applicants respectfully disagree. In particular, in the presently claimed invention, an outcome of the second instruction is a key into a software structure (e.g., a table) that includes a set of keys ("set of outcomes") determined earlier in the dependency chain (" second instruction") and a corresponding set of predicted outcomes of the first instruction. In Fu, in contrast, the table of predicted values referenced by the Examiner, does not contain a set of keys for different outcomes of a preceding instruction. Instead, the table in Fu consists of a set of predicted values, with each predicted value having a pair of commands ("LDPRED" and "UDPRED") accessed by the same table entry index. These LDPRED and UDPRED commands are used to load and update the predicted value in the register. Hence, the LDPRED and UPRED commands are not an equivalent to a set of keys claimed in claim 1.

Accordingly, Fu fails to disclose, teach, or suggest the limitation of amended claim 1 of determining that an outcome of the first instruction is dependent on an outcome of the second instruction based on the data flow graph, wherein the outcome of the second instruction represents a key into a software structure that includes a set of keys and a corresponding set of predicted outcomes of the first instruction.

Therefore, Applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103 (a) over Fu.

Because independent claims 14, 21, and 27 contain at least the limitation as discussed with respect to claim 1, Applicants respectfully submit that claims 14, 21, and 27 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu.

Given that claims 2-5, 15-18, 22-24, and 28 depend, directly or indirectly, from independent claims 1, 14, 21, and 27 respectively, and add additional limitations, Applicants respectfully submit that claims 2-5, 15-18, 22-24, and 28 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu.

Claims 6-9, 19, 25 and 29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over "Value Speculation Scheduling for High Performance Processors" by Fu et al. ("Fu") in view of U.S. Patent No. 6,308,322 of Serocki et al. ("Serocki").

Serocki discloses predicting indirect branch target addresses using target address hints in advance of their corresponding indirect branches. Hints comprising most-likely target addresses are generated using profile-based and/or rule-based heuristics (Serocki, col. 4, lines 28-42). Serocki, similarly to Fu, fails to disclose, teach, or suggest determining that an outcome of the first instruction is dependent on an outcome of the second instruction based on the data flow graph, wherein the outcome of the second instruction representing a key into a software structure that includes a set of keys and a corresponding set of predicted outcomes of the first instruction, as recited in claim 1.

Consequently, even if Fu and Serocki were combined, such a combination would lack such limitation of claim 1.

Therefore, applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103 (a) over Fu in view of Serocki.

Because independent claims 14, 21, and 27 contain at least the limitation as discussed with respect to claim 1, Applicants respectfully submit that claims 14, 21, and 27 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu in view of Serocki.

Given that claims 6-9, 19, 25 and 29 depend, directly or indirectly, from independent claims 1, 14, 21, and 27 respectively, and add additional limitations, Applicants respectfully submit that claims 6-9, 19, 25 and 29 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu in view of Serocki.

Claims 10-13, 20 and 26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over "Value Speculation Scheduling for High Performance Processors" by Fu et al. ("Fu") in view of U.S. Patent No. 6,687,807 of Damron ("Damron").

Damron discloses additional memory hardware to store and retrieve prefetch addresses while traversing linked data structures and, similarly to Fu and Serocki fails to disclose, teach, or suggest the limitation of claim 1 of determining that an outcome of the first instruction is dependent on an outcome of the second instruction based on the data flow graph, wherein the outcome of the second instruction representing a key into a software structure that includes a set of keys and a corresponding set of predicted outcomes of the first instruction.

Thus, neither Fu, Serocki, nor Damron discloses, teaches, or suggests such limitation of claim 1.

Consequently, even if Fu, Serocki, or Damron were combined, such a combination would lack such limitation of claim 1.

Therefore, applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103 (a) over Fu in view of Serocki and further in view of Damron.

Because independent claims 14, 21, and 27 contain at least the limitation as discussed with respect to claim 1, Applicants respectfully submit that claims 14, 21, and 27 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu in view of Serocki further in view of Damron.

Given that claims 10-13, 20 and 26 depend, directly or indirectly, from independent claims 1, 14, and 21 respectively, and add additional limitations, Applicants respectfully submit that claims 10-13, 20 and 26 are likewise not obvious under 35 U.S.C. § 103 (a) over Fu in view of Serocki and further in view of Damron.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Marina Portnova at (408) 720-8300.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: April 4, 2005

By: M. Portnova

Marina Portnova
Reg. No. 45,750

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(408) 720-8300